CLAIMS

1. A multi-level current pulse generator for driving the gates of a CMOS pair implemented using a low voltage process, comprising:

a multi-level pulse translator that generates a multi-level current pulse on each of at least one pulse node, each said multi-level current pulse having a first large current pulse with short duration followed by at least one smaller current pulse of longer duration and operative to switch the CMOS pair with reduced average power dissipation;

a current amplifier circuit having at least one input and a pair of outputs for coupling to the gates of the CMOS pair, each of said at least one input of said current amplifier circuit coupled to a corresponding one of said at least one pulse node; and

a clamp circuit for clamping gate voltage of the CMOS pair to prevent breakdown.

2. The multi-level current pulse generator of claim 1, wherein said multi-level pulse translator comprises:

a plurality of current sources;

a plurality of switches, each coupled to a corresponding one of said at least one pulse node and to a corresponding one of said plurality of current sources; and

a pulse timing circuit that controls said plurality of switches to generate a multi-level current pulse on each of said at least one pulse node.

3. The multi-level current pulse generator of claim 1, further comprising:

said at least one pulse node comprising a first pulse node and a second pulse node;

said multi-level pulse translator receiving a PWM signal having first and second states and generating a first multi-level current pulse on said first pulse node when said PWM signal is asserted to said first state and a second multi-level current pulse on said second pulse node when said PWM signal is asserted to said second state; and

said current amplifier circuit comprising a first current mirror amplifier having a first input coupled to said first pulse node and a second current mirror amplifier having a second input coupled to said second pulse node;

wherein each of said first and second current amplifiers have a pair of outputs for coupling to the gates of the CMOS pair for driving the CMOS pair into a first collective state in response to said first multi-level current pulse and into a second collective state in response to said second multi-level current pulse.

4. The multi-level current pulse generator of claim 3, the CMOS pair including a P-channel device and an N-channel device, further comprising:

said first current mirror amplifier operative to draw current from the gates of the P-channel device and the N-channel device to turn on the P-channel device and to turn off the N-channel device; and

said second current mirror amplifier operative to inject current into the gates of the P-channel device and the N-channel device to turn on the N-channel device and to turn off the P-channel device.

5. The multi-level current pulse generator of claim 4, the P-channel device coupled to a high voltage source and the N-channel device coupled to ground, wherein said clamp circuit comprises:

a pull-up clamp circuit, for coupling between the high voltage source and the gate of the P-channel device, operative to prevent the gate of the P-channel device from falling below a first voltage level; and

a pull-down clamp circuit, for coupling between ground and the gate of the N-channel device, operative to prevent the gate of the N-channel device from rising above a second voltage level.

6. The multi-level current pulse generator of claim 5, wherein:

said pull-up clamp circuit comprises:

a second N-channel device having a gate and having a drain and source coupled between the high voltage source and the gate of the P-channel device;

a first resistor-capacitor circuit coupled between the high voltage source and said gate of said gate of said second N-channel device; and

a first current source coupled to said gate of said second N-channel device; and

wherein said pull-down clamp circuit comprises:

a second P-channel device having a gate and having a drain and source coupled between ground and the gate of the N-channel device;

a second resistor-capacitor circuit coupled between ground and said gate of said gate of said second P-channel device; and

a second current source coupled to said gate of said second P-channel device.

7. The multi-level current pulse generator of claim 1, wherein said multi-level pulse translator and said current amplifier circuit generates an amplified multi-level current pulse to have a large first current pulse with a short duration, an intermediate second current pulse with an intermediate duration, and a third low current pulse with a long duration to minimize average power dissipation.

8. The multi-level current pulse generator of claim 7, wherein said first current pulse is sufficient to charge and discharge gate capacitance of the CMOS pair, wherein said second current pulse stabilizes gate voltage of the CMOS pair, and wherein said third current pulse provides a holding current level.

9. A high voltage gate driver implemented using a low voltage process, comprising:

a P-channel device and an N-channel device, each having a gate and each having a drain and a source coupled together at an intermediate junction and in series between high voltage source terminals;

a multi-level current pulse generator that provides at least one multi-level current pulse to said gates of said P-channel and N-channel devices sufficient to switch said P-channel and N-channel devices while minimizing average power dissipation; and

a clamp circuit coupled to limit gate to source voltage of said P-channel and N-channel devices to a predetermined maximum level.

10. The high voltage gate driver of claim 9, wherein:

said P-channel device comprises a PDMOS transistor having a source coupled to a high voltage source and a drain coupled to said intermediate junction; and

said N-channel device comprises an NDMOS transistor having a drain coupled to said intermediate junction and a source coupled to a reference node;

wherein said PDMOS and NDMOS devices are each implemented with an extended drain-to-source diffusion layer.

11. The high voltage gate driver of claim 10, wherein said clamp circuit comprises a first clamp circuit coupled to prevent said gate of said PDMOS transistor from dropping below a first voltage level and a second clamp circuit coupled to prevent said gate of said NDMOS transistor from rising above a second voltage level.

12. The high voltage gate driver of claim 11, wherein said low voltage process is a 5 Volt process, wherein said high voltage source is approximately 12 Volts, wherein said reference node is approximately zero Volts, wherein said first voltage level is approximately 7 Volts, and wherein said second voltage level is approximately 5 Volts.

13. The high voltage gate driver of claim 9, wherein said multi-level current pulse generator comprises:

a plurality of switched current sources;

a pulse timing circuit that controls said plurality of switched current sources to generate each of said at least one multi-level current pulse with a first large current pulse having a short duration and at least one additional reduced size current pulse; and

a current amplifier coupled to said plurality of switched current sources and to said gates of said P-channel and N-channel devices.

14. The high voltage gate driver of claim 13, wherein said pulse timing circuit turns on said plurality of switched current sources at a beginning of a PWM period and turns off said plurality of switched current sources one at a time during said PWM period to generate each of said at least one multi-level current pulse.

15. The high voltage gate driver of claim 13, wherein said multi-level current pulse generator generates a large first current pulse with a short duration, an intermediate second current pulse with an intermediate duration, and a third low current pulse during said PWM period.

16. The high voltage gate driver of claim 15, wherein said first current pulse is sufficient to charge and discharge gate capacitance of said P-channel and N-channel devices, wherein said second current pulse stabilizes voltage of said gates of said P-channel and N-channel devices, and wherein said third current pulse provides a holding current level.

17. The high voltage gate driver of claim 9, wherein said multi-level current pulse generator provides a first multi-level current pulse to turn on said P-channel device and to turn off said N-channel device and provides a second multi-level current pulse to turn on said N-channel device and to turn off said P-channel device.

18. The high voltage gate driver of claim 17, wherein said multi-level current pulse generator comprises:

a first current mirror amplifier that amplifies said first multi-level current pulse to pull current from said gates of said P-channel and N-channel devices; and

a second current mirror amplifier that amplifies said second multi-level current pulse to inject current into said gates of said P-channel and N-channel devices.

19. A method of driving a high voltage switching device using a gate driver implemented using a low voltage process, comprising:

generating at least one multi-level current pulse sufficient to modulate the gates of a P-channel device and an N-channel device with reduced average power dissipation; and

clamping the gates of the P-channel device and the N-channel device to predetermined voltage levels to prevent breakdown.

20. The method of claim 19, wherein said generating at least one multi-level current pulse comprises controllably switching a plurality of current sources.

21. The method of claim 20, wherein said controllably switching a plurality of current sources comprises activating multiple current sources at the beginning of a PWM period and turning off the current sources one by one.

22. The method of claim 19, wherein said generating at least one multi-level current pulse comprises generating a large first current pulse with a short duration, generating a successive intermediate second current pulse with an intermediate duration, and generating a successive third low current pulse with a long duration.

23. The method of claim 19, wherein said generating at least one multi-level current pulse comprises generating a first current pulse sufficient to charge and discharge gate capacitance, generating a second current pulse sufficient to stabilize gate voltage, and generating a third current pulse to provide a holding current.

24. The method of claim 19, wherein said generating at least one multi-level current pulse comprises amplifying current pulses using current mirrors.

25. The method of claim 19, wherein said generating at least one multi-level current pulse comprises:

generating a first multi-level current pulse;

applying the first multi-level current pulse to the gates of the P-channel and N-channel devices to turn the P-channel device on and to turn the N-channel device off;

generating a second multi-level current pulse; and

applying the second multi-level current pulse to the gates of the P-channel and N-channel devices to turn the P-channel device off and to turn the N-channel device on.

26. The method of claim 25, wherein said generating a first multi-level current pulse comprises generating the first multi-level current pulse in response to assertion of a PWM signal and wherein said generating a second multi-level current pulse comprises generating the second multi-level current pulse in response to de-assertion of the PWM signal.

27. The method of claim 19, wherein said clamping the gates of the P-channel device and the N-channel device comprises:

clamping the gate of the P-channel device from dropping below a minimum voltage level to prevent breakdown; and

clamping the gate of the N-channel device from rising above a maximum voltage level to prevent breakdown.